3.1 Hardware – Computer Architecture

ANSWERS

Question	Answer	Marks
1(a)	– A	1
1(b)	– C	1
1(c)	– Control unit	1
1(d)	Any **two** from: – (The CPU completes) 2.4 billion – … cycles/clock pulses **per second**	2
1(e)(i)	Any **two** from: – Stores data … – … that has been fetched/to be written to memory	2
1(e)(ii)	Any **three** from: – Memory address register // MAR – Program counter // PC – Current instruction register // CIR – Accumulator // ACC	3

Question	Answer	Marks
3(a)(i)	– The maximum number of FDE cycles/instructions a CPU can perform/process/execute in a second	1
3(a)(ii)	– Increases/improves the performance // Tasks can be performed quicker/faster – … because more FDE cycles/instructions can be processed in a second	2
3(b)	– **Stores** addresses … – … of next instruction/data to be fetched // where data is to be written to	2
3(c)	– Instruction set	1

Question	Answer	Marks
4(a)	Any **two** from: – Performs a single/limited/dedicated function/task – It has a microprocessor – It has **dedicated** hardware – Uses firmware – It is normally built into a larger device/system – User normally cannot reprogram – It does not require much power – It is cheap **to manufacture** – Works automatically // works without human intervention – It is small (in size) – It is a real-time system	2
4(b)	**One** mark for each correct system: – security light system – freezer – vending machine	3

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Question	Answer	Marks
3(a)	– Accumulator (ACC) – Control unit (CU) – Program counter (PC)	3
3(b)	Any **two** from: – It is a type of storage – …that stores **frequently used** data/instructions – To speed up **access** – … as it is faster to access than RAM – It has different levels e.g. L1 – L3	2
3(c)	– Clock	1
3(d)	– Arithmetic logic unit // ALU	1

Question	Answer	Marks
2(a)	Any **one** from: • To perform a fetch-decode-execute cycle • To **process** / **execute** an instruction	1
2(b)	**Two** from: • It may increase the performance • … because more instructions can be processed **simultaneously**	2
2(c)(i)	**Two** from: • To store / holds **data** / **address** / **instruction** • … temporarily	2

Question	Answer	Marks
2(c)(ii)	**One** mark for correct name of bus. **Two** marks for matching description. Address bus Transmit / carries addresses … … between **components** in the CPU Data bus Transmit / carries data … … between **components** in the CPU Control bus Transmits control signals … … from the **control unit** to other **components** in the CPU	3
2(d)	Any **two** from: e.g. • Keyboard // Keypad • Mouse • Touchscreen • Digital camera • QR code scanner • Barcode scanner • 2D scanner • Microphone	2
2(e)	• Any **one** from: • Speakers • Headphones	1
2(f)	• random access memory (RAM) • read only memory (ROM)	2

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Question	Answer	Marks
2(g)	Any **three** from: • Receives data from the self-checkout system • Compares the book data received to stored book data • … that is a **database** of stock • If the book is found it decrements the book stock by 1 • If the book is not found an error message is displayed	3

Question	Answer	Marks
2(a)	**One** mark for each correct bus (max 2) and **one** mark for corresponding description of transmission • Data bus • …. responsible for transmitting data/instructions • Control bus • … responsible for transmitting control signals	4
2(b)	Any **one** from: • Fetch • Decode	1
2(c)	Any **two** from: • To **temporarily** store data • It stores the **result** of interim **calculations** **One** from: • Arithmetic logic unit / ALU	3

Question	Answer	Marks
7	**One** mark for each correct term in the correct order • Fetched • MDR • Data bus • Decoded • ALU • Calculations • Execute	7

Question	Answer	Marks
2(a)(i)	• Random access memory // RAM	1
2(a)(ii)	**One** mark for each correct stage Second stage • Decode Third stage • Execute	2
2(a)(iii)	Any **two** from: • Memory address register // MAR • Memory data register //MDR • Program counter // PC • Control unit // CU • Address bus • Data bus • Control bus	2

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<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>6(a)</td><td>One mark per each correct row.

<table>
<tr><th>Statement</th><th>MAR (✓)</th><th>MDR (✓)</th><th>PC (✓)</th></tr>
<tr><td>it is a register in the CPU</td><td>✓</td><td>✓</td><td>✓</td></tr>
<tr><td>it holds the address of the next instruction to be processed</td><td>(✓)</td><td></td><td>✓</td></tr>
<tr><td>it holds the address of the data that is about to be fetched from memory</td><td>✓</td><td></td><td>(✓)</td></tr>
<tr><td>it holds the data that has been fetched from memory</td><td></td><td>✓</td><td></td></tr>
<tr><td>it receives signals from the control unit</td><td>✓</td><td>✓</td><td>✓</td></tr>
<tr><td>it uses the address bus to send an address to another component</td><td>✓</td><td></td><td>✓</td></tr>
</table></td><td>6</td></tr>
<tr><td>6(b)</td><td>– Arithmetic Logic Unit // ALU</td><td>1</td></tr>
</table>

Question	Answer	Marks
9(a)	Any **three** from: e.g. – A suitable description of any error that might occur – A peripheral is connected/disconnected – A key on a keyboard is pressed – A mouse button click – A phone/video call is received – A buffer requires more data – A printer has a paper jam – A printer runs out of paper – A printer runs out of ink – When switching from one application to another NOTE: If three suitable different errors are described, this can be awarded three marks.	3
9(b)	Any **one** from: – The computer would only start a new task when it had finished processing the current task // by example – Computer will not be able to multitask – Errors may not be dealt with – Computer would become impossible to use	1

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<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>5</td><td>One mark per correct term or description.

<table>
<tr><th>Component name</th><th>Description</th></tr>
<tr><td>Memory Address Register (MAR)</td><td>(A register that) holds the address of the data/instruction that needs to be fetched/processed // holds the address of where the data needs to be stored.</td></tr>
<tr><td>Program Counter (PC)</td><td>(A register that) holds the address of the next / current instruction to be processed.</td></tr>
<tr><td>accumulator // ACC</td><td>This is a register that is built into the arithmetic logic unit. It temporary holds the result of a calculation.</td></tr>
<tr><td>memory data register // MDR</td><td>This is a register that holds data or an instruction that has been fetched from memory.</td></tr>
<tr><td>Control Unit (CU)</td><td>Sends control signals to control the flow of data through the CPU // manages the execution of instructions in the CPU</td></tr>
<tr><td>address bus</td><td>This carries addresses around the CPU.</td></tr>
</table>
</td><td>6</td></tr>
</table>

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<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>10(a)</td><td>One mark per each correct row
<table>
<tr><th>Statement</th><th>ALU (✓)</th><th>CU (✓)</th><th>RAM (✓)</th></tr>
<tr><td>Stores data and instructions before they enter the central processing unit (CPU)</td><td></td><td></td><td>✓</td></tr>
<tr><td>Contains a register called the accumulator</td><td>✓</td><td></td><td></td></tr>
<tr><td>Manages the transmission of data and instructions to the correct components</td><td></td><td>✓</td><td></td></tr>
<tr><td>Contained within the CPU</td><td>✓</td><td>✓</td><td></td></tr>
<tr><td>Uses the data bus to send data into or out of the CPU</td><td>(✓)</td><td></td><td>✓</td></tr>
<tr><td>Carries out calculations on data</td><td>✓</td><td></td><td></td></tr>
</table></td><td>6</td></tr>
<tr><td>10(b)</td><td>Any two from:
– MAR
– MDR // MBR
– PC
– CIR // IR</td><td>2</td></tr>
</table>

Question	Answer	Marks
8(a)	– **Instructions** and **data** stored in the same/main memory – Instructions fetched and executed in order / one after another / in sequence	2
8(b)(i)	– Holds the **address** … – … of **next** / **current** instruction	2
8(b)(ii)	Any **two** from: – Carries / transfers **control** signals/instructions // carries/transfers commands … – … from CPU/CU to components // from devices to CPU/CU – To synchronise the FE cycle	2
8(c)	Any **two** from: – To identify that the processor's attention is required // to stop the current **process/task** – To allow multitasking – To allow for efficient processing // prioritising actions – To allow for efficient use of hardware – To allow time-sensitive requests to be dealt with – To avoid the need to poll devices	2